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**REMARKS****Claim Rejections Under 35 U.S.C. § 102**

Claims 9, 13, 18, 20, and 22 were rejected as being anticipated by *Imamiya et al.* (U.S. Patent No. 6,031,764).

Claims 9, 13, 18, 20 and 22 have been amended to more clearly claim the subject matter that Applicant regards as the invention. Claims 9, 13, 18, 20 and 22 have been amended to include limitations regarding the voltage applied to the different wells of each memory block. Claims 10, 14, 19, and 21 have been canceled without prejudice to avoid duplicate claiming.

*Imamiya et al.* disclose a nonvolatile semiconductor memory device that has memory blocks formed in wells formed separately in a semiconductor substrate. *Imamiya et al.* neither teach nor suggest the voltage differential between different wells.

Additionally, during an erase operation, *Imamiya et al.* uses a voltage of 0V on the Well A or Well B control terminals (see col. 7, lines 27 – 38 and col. 8, lines 10 – 26). Applicant's claims for the erase operation, claims 20 and 21, claim a voltage differential of 5V between the two wells (i.e., claims 9, 13, 18, and 22) or a voltage of -5V (i.e., claim 20) for the unselected array block wells. These limitations are neither taught nor suggested by *Imamiya et al.*

During a program operation, *Imamiya et al.* disclose using 0V on the Well A or B control terminal for an unselected NAND block (see col. 10, lines 21 – 31). Applicant claims using a voltage that is greater than 0V on unselected second conductivity material to isolate the unselected array blocks. *Imamiya et al.*, therefore, teaches away from Applicant's claimed invention.


**CONCLUSION**

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

Date: \_\_\_\_\_

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